ABSTRACT OF THE DISCLOSURE

A method is provided for processing a semiconductor topography such that its upper surface is substantially planar, particularly including a region adjacent to an outer edge of a semiconductor topography. The method may include preferentially removing a portion of an upper layer of the topography in a region adjacent to an outer edge of the semiconductor topography. The region may extend greater than approximately 3 mm inward from the outer edge of the semiconductor topography. The method may also include polishing the semiconductor topography such that the upper surface of the semiconductor topography is substantially planar. Therefore, although a rate of polishing adjacent to an outer edge of the semiconductor topography may be slower than a rate of polishing adjacent to a center of the semiconductor topography, a thickness variation of the polished upper layer across the entirety of the semiconductor topography may be less than approximately 500 angstroms.